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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/926,489	12/14/2001	Binh Vu Thien	01196	6690

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EXAMINER	
ROY, SIKHA	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,489	THIEN ET AL.	
	Examiner	Art Unit	
	Sikha Roy	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The Amendment, filed on September 1, 2004 has been entered and is acknowledged by the Examiner.

New claims 19 and 20 have been entered.

The new drawing of Fig. 11 has been entered and is approved by the examiner.

Specification

The disclosure is objected to because of the following informalities:

Page 5 after line 27, brief description of the drawing of Fig. 11 should be inserted.

The title of the invention is not correct. In the title 'extraction of electrodes' should be changed to --extraction of electrons--.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-16 and 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over WO 98/06135 to Shannon et al. in view of U.S. Patent 6,635,979 to Shiratori et al. and further in view of U.S. Patent 3,964,084 to Andrews et al.

Regarding claim 1 Shannon discloses (Fig. 1, page 7 lines 1-10,17-30) a method of extracting electrons in vacuum 105 from the cathode comprising emitter array 50 situated in spaced-apart relationship with an anode 101 which is placed at a given potential relative to the cathode comprises making cathode presenting one junction 12 between metal 14 (injector electrode formed of chromium) serving as reservoir of electrons and an n-type semiconductor film 10, the cathode presenting an electron emission surface 11a having a surface potential barrier of about 0.85 ev and the semiconductor film having a thickness of 100nm (0.1μm) (page 8 lines 19-24). The electrons emitted from the metal electrode 14 and injected through the metal/semiconductor junction 12 create charge in the semiconductor lowering the surface potential barrier of the emission area 11a resulting in electron emission in to the vacuum 105. Shannon discloses (page 5 lines 24 through page 6 line 1) that positive bias on the anode provides electron-accumulation means which induces accumulation of electrons at the emission surface area of the semiconductor film facing vacuum gap. Hence controlling the bias the height of the surface potential barrier of the semiconductor film is modified controlling the electron emission flux.

Claim 1 differs from Shannon in that Shannon fails to disclose the thickness of the n-type semiconductor film lying in the range 1nm to 20nm.

Shiratori in analogous art of electron emitting device discloses (column 27 lines 40-54, Fig. 15) an electron emitter comprising an electron injection electrode 101, an electron transporting member 102 formed of diamond thin film of thickness 1 nm or more formed in contact with the electrode 101. It is to be noted that this thickness of the

diamond film provides desired electron affinity of the film for efficient electron injection into vacuum.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify the thickness of the n-type semiconductor film of the emitter of Shannon to thickness of 1nm or more as taught by Shiratori for providing desired electron affinity for efficient emission of electrons.

Shannon and Shiratori does not disclose the surface potential barrier with a height in a range of .05 to .5 ev.

Andrews in pertinent art of Schottky barrier diode discloses (column 1 lines 50-60, column 2 line 44 through column 3 line 6) by changing the carrier concentration of the n-type semiconductor and the thickness of the implanted layer, the barrier height can be modified to about 0.6ev. Andrew further discloses (column 3 lines 20-27) that this reduction of barrier height results in increased current flow.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify the thickness and carrier concentration of the semiconductor forming the junction with metal in the cathode of Shannon and Shiratori as suggested by Andrews to have the potential barrier height of 0.6ev in order to have increased current flow and hence an improved cathode.

Regarding claim 1, Shannon, Shiratori and Andrews disclose the claimed invention except for the limitation of range of the barrier height of .05 to 0.5 ev. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re*

Aller, 105 USPQ 233. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the barrier height in the range of .05 ev to .5 ev by controlling the carrier concentration in the n-type semiconductor and selecting particular semiconductor material forming the junction with metal for increasing flow of electrons and the current from the cathode, since optimization of workable ranges is considered within the skill of the art.

Claim 6 essentially recites the same limitations of method of extracting electrons of claim 1 for the device for extracting electrons and hence is rejected for the same reason.

Regarding claim 2 Shannon discloses (Fig. 4 page 10 lines 5-15,25,26) the bias source (difference in potential of the anode (front electrode) compared to the injector electrode 14) is provided so that the barrier present between the injector electrode and the semiconductor film 10 prevents injection of current of electrons into the film (height of the surface potential barrier of the semiconductor is greater than the level of states occupied by the electrons) and no electrons are emitted.

Regarding claim 3 Shannon discloses (page 8 lines 1-11) the potential bias between the anode and the injector electrode controls the height of the surface potential of the emission area 11a of the semiconductor and controls the magnitude of electron accumulation layer Ne in the semiconductor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify the bias of the emitter array of Shannon such that the potential barrier height is equal to the level of states of

occupied electrons in the semiconductor with predetermined affinity for facilitating emission of electrons.

Regarding claim 4 Shannon discloses (Fig. 3 page 10 lines 3-5, 11-20) that when bias is controlled such that the height of the potential barrier of n-type semiconductor is lower than the level of states occupied by electrons in the semiconductor, electrons emit from the surface area 11a.

Regarding claim 7 Shannon discloses the device (Fig. 1) including an extraction electrode (front electrode) 15 followed by an anode 102 for receiving the extracted electrons.

Claim 8 essentially recites the same limitations of claim 6 for electron emission cathode and hence is rejected for the same reason (see rejection of claim 1).

Regarding claim 9 Shannon, Shiratori and Andrews disclose the claimed invention except for the limitation of range of the barrier height of approximately 0.1 ev. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the barrier height in the range of .1ev by controlling the carrier concentration in the n-type semiconductor and selecting particular semiconductor material forming the junction with metal for increasing flow of electrons and the current from the cathode, since optimization of workable ranges is considered within the skill of the art.

Regarding claim 10 Shannon discloses (Fig. 1 page 7 lines 11-17) the emitters characterized in that the first portion forming an electron reservoir formed by metal layer (injector electrode) 14 carried on a substrate 5 made of glass or any insulating material.

Regarding claim 11 Shannon discloses (Figs 1, 5) the n-type semiconductor 10 possesses an emission surface area 15 that is substantially plane.

Regarding claims 12,13 and 14 Shiratori in Fig. 15 discloses the semiconductor (electron transporting member) 102 possessing an emission surface that presents projections.

In claim 12 the recitation of 'enabling electron emission to be confined' is functional language and has not been given patentable weight because it is narrative in form.

In claims 13 and 14 the Examiner notes that the claim limitation that "made by lithographic techniques (claim 13) and obtained by ion bombardment (claim 14)" are drawn to a process of manufacturing which is incidental to the claimed apparatus. It is well established that a claimed apparatus cannot be distinguished over the prior art by a process limitation. Consequently, absent a showing of an unobvious difference between the claimed product and the prior art, the subject product-by-process claim limitation is not afforded patentable weight (see MPEP 2113). Therefore, it is the position of the examiner that it would have been obvious to one of ordinary skill in the art that the emitter array disclosed by Shannon and Shiratori is at least a fully functional equivalent to the Applicant's claimed invention as evidenced by all of the Applicant's claimed structural limitations.

Referring to claim 15 Shiratori discloses (Fig. 22 (a), 22(b) column 11 lines 10-14 column 16 lines 31-33, 60-65) the first portion forming electron reservoir constituted by metal (conductive) layer 1 carried by a semiconductor substrate 11 having active components (SiO_2 layer) 2 arranged for controlling electron emission.

Regarding claim 16, Shannon and Shiratori disclose the claimed invention except for the limitation of substrate possessing point or pinhead shape. It has been held that a change in shape is generally recognized as being within the level of ordinary skill in the art. It would have been obvious to one having ordinary skill in the art to modify the substrate having point shape, since such a modification would have involved a mere change in the shape of a component.

Claims 19 and 20 essentially recite the same limitation as of claim 9 and hence are rejected for the same reason (see rejection of claim 9).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over WO 98/06135 to Shannon et al., U.S. Patent 6,635,979 to Shiratori et al. and U.S. Patent 3,964,084 to Andrews et al. and further in view of U.S. Patent 3,114,070 to Stratton.

Regarding claim 5 Shannon, Shiratori and Andrews are silent about controlling the temperature of cathode to control the flux of electron emission.

Stratton in same field of endeavor of electron emitters discloses (column 2 lines 13-15,35-40) moderate heating leads to increased electron densities and hence a very large emission current from the surface of semiconductor cathode.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify the temperature of the cathode of Shannon, Shiratori and Andrews for increasing emission current.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 5, 243,197 to Van Gorkom et al. and U.S. Patent 6,417,606 to Nakamoto et al. disclose emitter cathode with semiconductor and metal junction.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sikha Roy whose telephone number is (571) 272-2463. The examiner can normally be reached on Monday-Friday 8:00 a.m. – 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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